Toroidal Inductors for Integrated Radio Frequency and Microwave Circuits

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Abstract—
A toroidal inductor has been developed that confines flux and eliminates eddy currents. A printed circuit and micromachined RFIC-compatible implementations of the inductor are presented.

I. Introduction

LUMPED inductors are essential elements in RFICs and Microwave Monolithic Integrated Circuits. They are used in lumped element matching networks where transmission line structures may be of excessive length. More commonly they are used as RF chokes allowing bias currents to be supplied to circuits while providing broadband high impedance at RF frequencies and above. They are also used to ensure stability at frequencies below the frequencies of operation — a function that can not be realized using transmission line sections. Lumped inductors embedded in packaging, for example in LTCC circuitry, and in traditional circuit board laminates are also used with the same properties. Traditionally high frequency lumped inductors are realized as spiral inductors such as that shown in Figure 1.

Inductors of up to 10 nH can be fabricated on-chip. Values above this consume too much die area and either the entire inductance, or the majority of a required inductance, are fabricated off-chip, more often on an LTCC substrate or as part of the RFIC package. With care, reasonably good inductors, with high Q, can be realized on GaAs chips as the GaAs substrate is semi-insulating. The situation is different with silicon because of the finite conductivity of silicon substrates, which therefore supports eddy currents.

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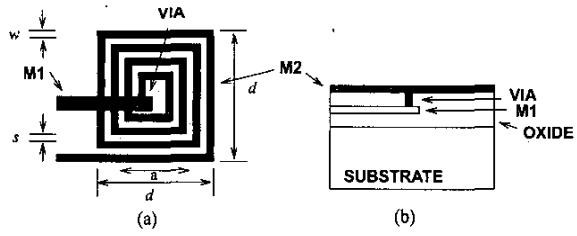

Fig. 1. An on-chip spiral inductor: (a) plan view; and (b) side view.

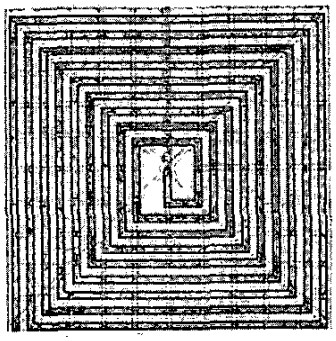

Fig. 2. An on-chip spiral inductor with tesselated ground shield to reduce eddy current effects.

One of the major sources of inductor loss inductors on silicon substrate is due to the finite conductivity of the substrate and the resulting induced current flow. These induced currents follow a path under the conductors of the spiral and, just as with ground plane eddy currents, lower the inductance achieved. Eddy currents are also excited in the metal backing of dies and package metallization. These however can be mitigated using a tesselated ground shield that largely eliminates eddy current flow in metallization since there are current paths, see Figure 2. Most silicon substrates are at least slightly doped, usually of p-type. Thus heavily doped n-type strips arranged radially from the center axis of the spiral, act to block eddy currents. They achieved an increase of the Q from 5.3 to 6.0 at 3.5 GHz and from 4.3 to 4.5 at 2.0 GHz [1]. In the spiral inductor model, the effect was also to reduce the shunt resistance and capacitance to the substrate.

Other state-of-the-art results achieved are represented by the work of Bahl *et al.* [2] for a spiral inductor on GaAs obtaining a Q of 44 at 11.5 GHz; Burghartz *et al.* [4] used multiple level interconnects in parallel on silicon achieving a Q of 24 at 2.3 GHz; Dekker *et al.* [6]implemented an aluminum spiral inductor on a glass substrate achieving a Q of 39 at 4.3 GHz; and Park *et al.* [7] obtained a Q of 15.3 using an aluminum spiral inductor on high resistivity silicon. Other important results include a suspended aluminum spiral inductor by Sun *et al.* obtaining a Q of 28 at 4.3 GHz; and a suspended 1.5 μm thick copper spiral inductor by Jiang and Wang [9]. A more complete tabulation is given in Reference [10].

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Parasitic capacitance results in resonance of the on-chip inductance structure and hence limit the frequency of operation. With GaAs ($\varepsilon_r = 12.85$) the effective permittivity of the medium can be reduced by adding a polyimide layer ($\varepsilon_r = 3.2$) and using metallization on top of this layer [2]. With thick metallization to reduce resistance, a Q that is 50% larger and a self-resonant frequency that is 25% higher [2] can be obtained. The specific results are

We now return to the issue of the finite conductivity of the silicon substrate. The inducement of charges in the silicon and the insignificant skin depth of the silicon substrate has the effect of increasing the capacitance of an interconnect line over silicon as the electric field lines are terminated on the substrate charges. (This effect is in addition to the induction of eddy currents in the substrate.) Now the magnetic field lines penetrate some distance into the substrate so that the LC product is greater than if the substrate was insulating (as with GaAs). The effect is that the velocity of propagation along the interconnect ($= 1/\sqrt{LC}$) is reduced, leading to what is called the slow wave effect.

The lowest loss inductors are obtained by etching away the underlying substrate or by using insulating or very high resistivity bulk material. Loss is also reduced by separating the planar inductor from the ground plane and additional dielectric layers have been deposited on a chip to achieve this. Volant and Groves [11] obtained a Q of 18 at 10 GHz with a 4 μm thick aluminum-copper spiral inductor using this approach. When all steps have been taken then the dominant loss mechanism is current crowding [13]. This is a particular problem with multi-turn spiral inductors which are required to realize high inductance values. Current crowding results when the magnetic field of one turn penetrates an adjacent trace creating eddy currents so that current peaks on the inside edge of the victim trace (towards the center of the spiral) and reduces on the outside edge. This constricts current and results in higher resistance than would be predicted from skin effect and DC resistance alone [13]. In summary the best that can be achieved for conventional spiral inductors on low resistivity silicon is around 6 with a self resonant frequency of 3.5 GHz [10].

The key issue with controlling the Q of inductors is confining the magnetic flux lines to a defined path and ensuring that they do not intersect with metals and semiconducting materials where they would induce eddy currents. This results in additional losses and lower inductance values since the eddy currents reduce flux coupling. Our proposed toroidal inductor 3 confines the magnetic fields and maintains high flux linkage. The toroidal inductor was fabricated first on a microwave printed circuit board and then fabricated on a silicon wafer using micromachining.

II. Printed Wiring Board Implementation

A printed wiring board (PWB) implementation of the concept was realized with the structure is shown in Figure 3. The measured and calculated reflection coefficient of the structure is shown on a Smith chart in Figure 4. The

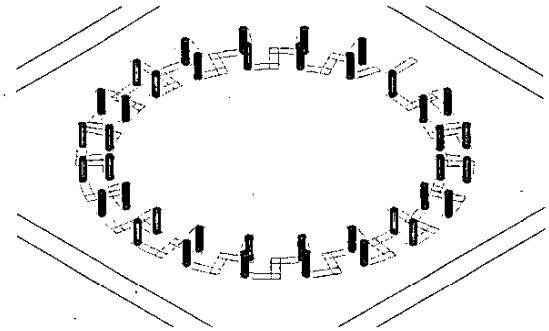

Fig. 3. Printed circuit board implementation of the toroidal inductor.

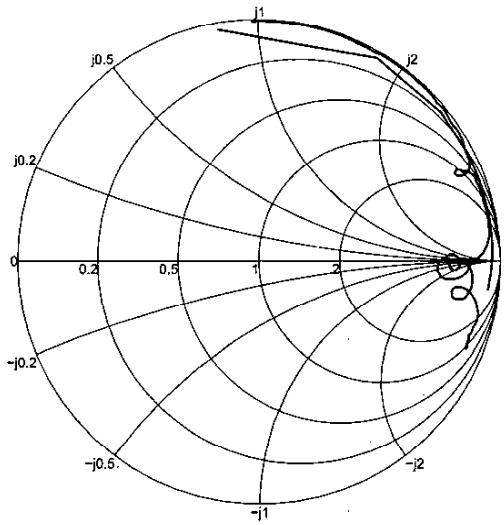

Fig. 4. Smith Chart showing measured and simulated S_{11} for the PWB structure.

locus is very close to the unit circle of the Smith indicating both a high Q and also great reliance on the integrity of the calibration procedure. The possible transmission line like behavior of the inductor is investigated in Figure 5 where the phase variation is in line with an inductance and not a transmission line. The inductance of this structure was obtained from the measured reactance and is shown in Figure 6. A low frequency inductance of 0.95 nH was obtained.

The structure was also simulated using Agilent Technologies HFSS Em simulator yielding a peak Q of 40 and a low frequency inductance of 0.8 nH compared to a measured low frequency inductance of 0.95 nH. The measured peak Q was very large, greater than 40, and the traditional reflection coefficient procedure could not be used to determine a reliable value but did establish the minimum Q.

III. Micromachined Implementation

The micromachined implementation of the toroidal inductor utilizes a fabrication procedure for realization of a suspended structure (a metal bridge in this case) on a pro-

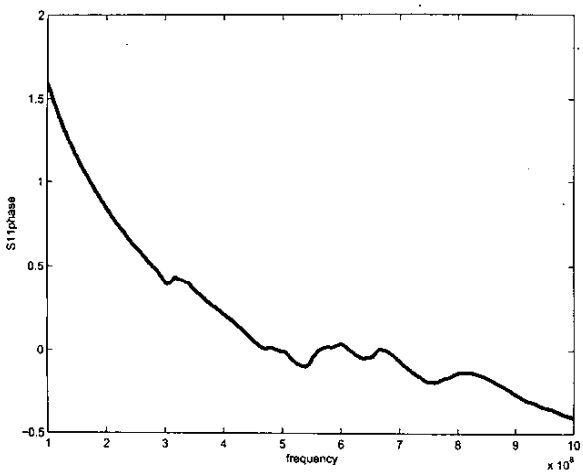

Fig. 5. S_{11} phase versus frequency measurement for the PCB structure.

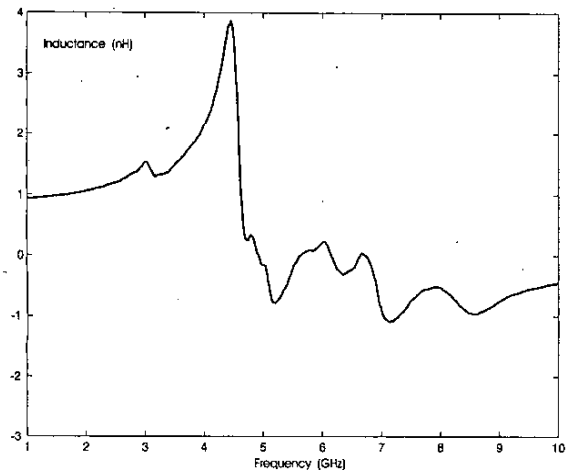

Fig. 6. Measured effective inductance versus frequency for the PWB toroidal inductor.

cessed silicon wafer. In this process, the anchoring points are fabricated together with the turns of the inductor, as opposed to other techniques that necessitate separate steps for fabrication of anchoring points to obtain the same air bridge functionality.

The toroidal inductor was fabricated on a low resistivity (20 Ω.cm) silicon substrate with a thickness of 500 μm. The backside of the substrate was effectively grounded during measurements The intent here was to target a substrate typical of current bulk CMOS technology. The inductors could have just as easily been fabricated on high resistivity silicon. However our concept of flux confinement to the region defined by the successive coils should minimize eddy current flow in the low resistivity silicon. One coil of the inductor is shown in Figure 7. A photograph of the completed structure is shown in Figure 8 and it has an outer

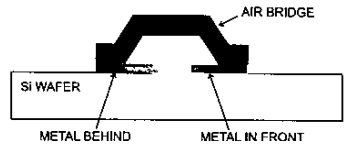

Fig. 7. Coiled cross section showing air bridge constructed using micromachining.

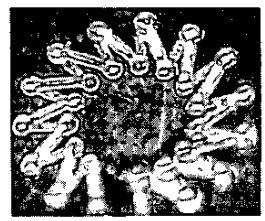

Fig. 8. Toroidal inductor fabricated on a silicon wafer.

diameter of 1 mm.

The steps in the fabrication process are as follows:

Step 1: To start with, the metal strips representing the input/output lead lines and the bottom segments of the inductor are photolithographically defined and metallized by either evaporation or ion-sputtering, with preferably chromium and then gold.

Step 2: A layer of thick photoresist is deposited onto the wafer, with the thickness of the photoresist defining the height of the metal bridge.

Step 3: The anchoring points are photolithographically patterned onto the layer of photoresist deposited in Step 3.

Step 4: Then, another layer of gold or gold/palladium is ion-sputtered on the top of the photoresist that defines the anchoring points.

Step 5: Another thin layer of photoresist defining the metal bridges is photolithographically patterned, forming the etch-mask for the suspended bridges.

Step 6: The bridges of the inductor are etched off using a suitable gold etchant. The photoresist formed in Step 6 is then exposed under UV light and developed. The metal layer representing the metal bridges of the inductor is then thickened significantly by electroplating.

Step 7: The photoresist that remains in the wafer is stripped off using acetone. The remaining residues of the photoresist that remain in the wafer can be etched away by oxygen plasma. This procedure results in the suspended bridge for the toroidal inductor as illustrated in Figure 8.

The measured reflection coefficient characteristic of the toroidal inductor is shown in Figure 9 and the effective inductance and Q are shown in Figure 10. The effective inductance is 1.9 nH with a peak Q of 9.6. This structure shows loss and these are attributed to eddy currents due to the residual magnetic flux lines that are not confined within the coil of the toroid.

IV. Conclusion

This paper introduced the toroidal inductor as a potentially high performance candidate for use in RF and mi-

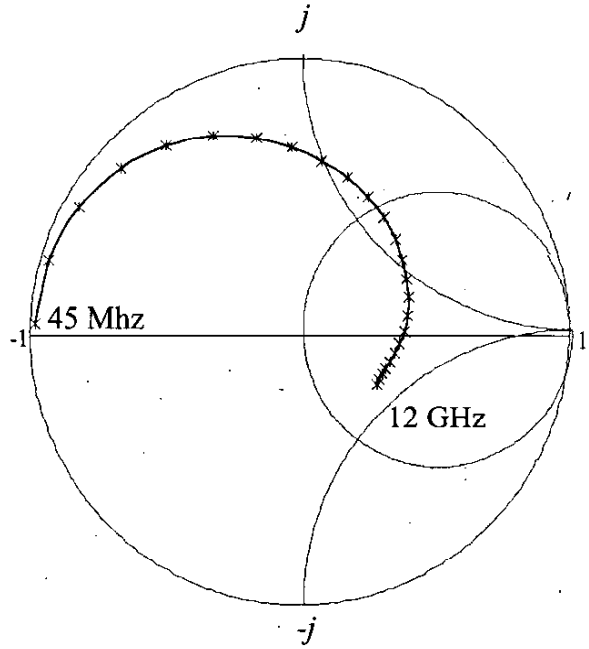

Fig. 9. Measured reflection coefficient of the micromachined toroidal inductor.

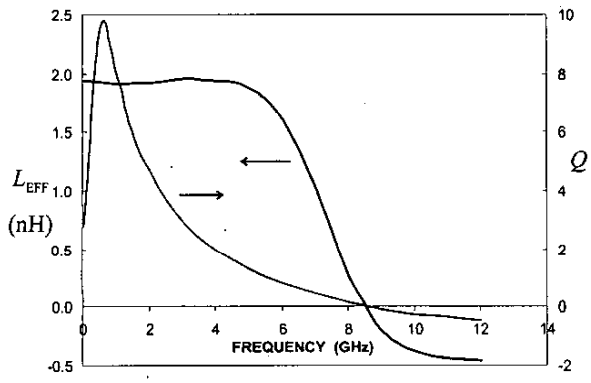

Fig. 10. Measured effective inductance and Q of the micromachined toroidal inductor.

crowave circuits on-chip or in-package. The key aspect of the inductor is confinement of the magnetic flux lines within the coil region thus reducing eddy currents that can be induced in the substrate and metallization.

Acknowledgement

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References

[1] Mernyei, F., Darrer, F., Pardoen, M. and Sibrai, A., 'Reducing the substrate losses of RF integrated inductors,' *IEEE Microwave Guided Wave Lett.*, Vol. 8, No. 9, Sept. 1998, pp. 300–301.

[2] Bahl, I. J., 'High current handing capacity multilayer inductors for RF and microwave circuits,' *Int. J. RF and Microwave Computer-Aided Engineering*, Vol. 10, No. 2, March 2000, pp. 139–146.

[3] Burghartz, J. N., 'Spiral inductors on silicon — status and trends,' *Int. J. of RF and Microwave Computer-Aided Engineering*, Vol. 8, No. 6, Nov. 1998, pp. 422–432.

[4] Burghartz, J. N., Soyuer, M., Jenkins, K. A. and Hulvey, D., 'High-Q inductors in standard silicon interconnect technologies and its application to an integrated RF power amplifier,' *Tech. Dig. Int. Electron Devices Meeting*, 1995, pp. 1015–1017.

[5] Burghartz, J. N., Jenkins, K. A. and Soyuer, M., 'Multilevel-spiral inductors using VLSI interconnect technology,' *IEEE Electron Device Lett.*, Vol. 17, No. 9, 1996, pp. 428–430.

[6] Dekker, R., Baltus, P., van Deurzen, M., v.d. Einden, W., Maas, H. and Wagemans, A., 'An ultra low-power RF bipolar technology on glass,' *Tech. Dig. Int. Electron Devices Meeting*, 1997, pp. 921–923.

[7] Park, M., Kim, C. S., Park, J. M., Yu, H. K. and Nam, K. S., 'High Q microwave inductors in CMOS double-metal technology and its substrate bias effects for 2 GHz RF ICS application,' *Tech. Dig. Int. Electron Devices Meeting*, 1997, pp. 59–62.

[8] Sun, Y., van Zeijl, H., Tauritz, J. L. and Baets, R. G. F., 'Suspended membrane inductors and capacitors for application in silicon MMIC's,' *1996 IEEE MTT-S Int. Microwave Symp. Dig.*, June 1996, pp. 99–102.

[9] Jiang, H., Wang, Y., J.-L. A. and Tien, N.C., 'Fabrication of high performance on-chip suspended spiral inductors by micromachining and electroless copper plating,' *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, June 2000, pp. 279–282.

[10] Edwards, T. C. and Steer, M. B., Chapter 10 in *Foundatiosn of Interconnect and Microstrip Design*, John Wiley & Sons, 2000.

[11] Volant, R., Malinowski, J., Subbanna, S. and Begle, E., 'Fabrication of high frequency passives on BiCMOS silicon substrates,' *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, June 2000, pp. 209–212.

[12] Yamaguchi, M., Baba, M., Suezawa, K., Moizumi, T., Arai, K. I., Shimada, Y., Haga, A., Tanabe, S. and Ito, K., 'Magnetic RF integrated thin-film inductors,' *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, June 2000, pp. 205–208.

[13] Kuhn, W. B., 'Approximate analytical modeling of currrent crowding effects in multi-turn spiral inductors,' *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, June 2000, pp. 405–408.

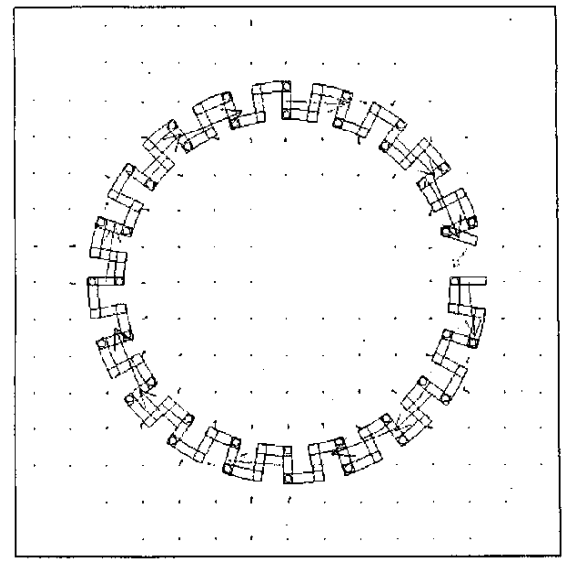

Fig. 11. Magnetic flux lines of the toroidal inductor.